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|---|
| TRIMMINGS, JOHN P |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/846,374 | TALAGALA ET AL. | |
| | Examiner | Art Unit | |
| | John P Trimmings | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *4/30/2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

Claims 1 – 60 are presented for examination.

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG. 3d, 328a, 328e, 322a, 322e, and 326. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because FIG. 4b, box 407 contains the reference "FIG. 4b", and the examiner believes that the reference should be "FIG. 4c". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because FIG. 4b, box 409 contains the reference "FIG. 4c", and the examiner believes that the reference should be "FIG. 4d". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because FIG. 4b, box 410 contains the reference "FIG. 4d", and the examiner believes that the reference should be

"FIG. 4e". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG. 4c, 411. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG. 4d, 421. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to because FIG. 4d, 428 appears to the examiner to be in error where "first" most likely should be "second". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to because FIG. 4d, 433 contains confusing information not part of claim 14; the only function claimed is creation of a restored 2nd checksum to replace the corrupted 2nd checksum. A proposed

drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG. 4e, 441. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

10. The disclosure is objected to because of the following informalities: Paragraph [0053] refers to "RAID 1" system in FIG. 4d (line 2), but the examiner believes that FIG. 4d is a RAID 5 system example, and was previously referred to in a RAID 5 methodology in the content of paragraph [0042]. Instead of referring to the same figure as RAID 1 and RAID 5, which is confusing, the examiner suggests that there be two distinct drawings. Appropriate correction is required.

11. The disclosure is objected to because of the following informalities: Paragraph [0054] references a RAID 5 example FIG. 4d in order to explain a RAID 1 methodology, which is confusing and misleading to the examiner. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187.

15. As per claim 1:

Hong et al., in patent column 35 lines 63-68, and column 36 lines 1-27 substantially teaches the method of arranging the data signals, generating check redundancy signals, with a 1st set of checks bits (CRC type), a 2nd set of parity check bits, storing the data as digital signals, and then detecting an error in at least one of the signals (see also the abstract in Hong et al.). Hong et al. bases the error correction on a horizontal to vertical redundant relationship (column 2 lines 38-48) of bytes and bits. However, the Hong et al. teaching does not specifically point out the data

size to be block-size. Hong et al. applies this method to bytes, where the applicant applies the method to data blocks. However, it would have been obvious to one with ordinary skill in the art at the time of the invention to apply the byte-wise method of Hong et al. to create a data block method. One would have been motivated, in order to provide multiple block correction capability as set forth in Hong et al., to copy the completely compatible method of Hong et al., applying this vertical and horizontal redundancy to error correction to a block-wise method such as in the applicant's claim.

16. As per claim 2:

Hong et al. substantially teaches calculating new checksum signals and comparing it to the stored signals in the following: "...taking transferred signals and generating new first and second check redundancy signal bytes..." (column 36 lines 18-19), and "...evaluating signal transfer and pointing to bytes possibly in error..." (column 36 lines 29-30...). Hong et al. applies this method to bytes, where the applicant applies the method to data blocks. However, it would have been obvious to one with ordinary skill in the art at the time of the invention to apply a byte-wise method to a data block. One would have been motivated to do so, in the specification of a data-block method, to copy the completely compatible method of Hong et al. in order to apply vertical and horizontal redundancy to error correction.

17. As per claim 3:

Claim 34 of Hong et al. substantially teaches the vertical and horizontal redundancy relationships of the signals, and their overall relationship with each other (column 2 lines38-44). However, Hong's teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical (see Figures 2 and 3 in Hong et al.). One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. teachings. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 36 lines 51-68 of Hong et al. fully describes a method of "...reading correcting errors in digital signals..." which generates a 1st set of check bits (CRC) with a redundant relationship to each of a plurality of channels, and generating 2nd check signals having a parity relationship with single frames of data, each frame a part of a plurality of frames, the parity also having a redundant relationship to the CRC check signal. The relationship of the 1st to the 2nd checks is that of a vertical and horizontal nature to the data (column 2 lines 38-44 of Hong et al.). When reading data, the CRC and parity bits are recomputed on the incoming data, and compared with the incoming CRC and parity, and failing data are identified based on unequal comparisons. When comparing check signals, Hong et al. says that the

checksum can be reconstructed based on locating the error in the checksum (column 36 lines 62-68 and column 37 lines 1-5). However, Hong's teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time of the invention, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Claim 38 of Hong et al. fully describes a method of detecting and correcting more than one error in more than one track, in column 15 lines 54-64. In other words, all blocks are reviewed for errors and more than one byte can be pointed out. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

20. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 36 lines 16-27 of Hong et al.

fully describes a method of "...taking transferred signals and generating new first and second check redundancy signal bytes therefrom..." In other words, a new parity relationship is generated. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

21. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 5 lines 52-56 of Hong et al. fully describes a method of reading correcting signals in digital signals, calculating parity and CRC, and if there is an error, pointing to the data in error, and correcting the data associated with the check signal. This applies to checksums in error as well as data in error (column 36 lines 62-68 and column 37 lines 1-6). In claim 8 of the applicant above, the applicant indicates a checksum correction. However, Hong's teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to

block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

22. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187, and further in view of Sawao Iwatani, U.S. Patent No. 6023780. In Iwatani's patent, it teaches data read controlling means for comparing the data read from two disk drives and then restructuring data when the data are mismatched. This identifies the method used to detect errors in two drives is comparison of the data in the two drives directly (see Iwatani column 5 lines 24-56). The combination of the two patents above serves to encompass the applicant's claim 7.

23. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187, and further in view of Sawao Iwatani, U.S. Patent No. 6023780. In Iwatani's patent, column 5 lines 49-52 teaches restructuring the data based on the first parity and valid part of the data. The restructured data is then validated in Iwatani column 5 lines 52-56, wherein a cyclic redundancy check is used to validate the restructured data. The combination of Hong and Iwatani completely covers all of the points of the applicant's claim.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187, and further in view of Ng et al., U.S. Patent No. Re. 36846. Column 5 lines 52-57 of Hong et al. teaches showing which signals in such group are in error; and changing the signals in error. This claim of Hong et al., while not specifically teaching the replacement of the

checksum, shows that the checksum (or parity) may be replaced if it is determined to be in error, because the correction has that capability. In RAID systems, replacement of entire blocks because of errors is a common occurrence, and checksums are blocks of data. In Ng et al., Figure 11 and column 1 lines 61-68, the method detects the error, identifies the faulty location, rebuilds the data, and then re-writes the corrected data. If one skilled in the art at the time of the invention were storing data, parity, and checksums, then the re-writing of data would encompass all three parts of the system, including checksums. The combination of these two inventions would have made it obvious.

25. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. In the Hong et al. patent, column 15 lines 53-64 describes the process of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also infers that if there were no parity indicators to rely on, correction of checksums would not occur (column 39 lines 47-50 of Hong et al.). Since there would be no correction without the use of parity bits, the data loss error would remain as an error condition, and would be reported to the system. One with ordinary skill in the art at the time of the invention would see that the error condition would remain active, and the data would remain uncorrected, if the parity indicators were showing "good" data. If one skilled in the art were to create a flow chart of a dual CRC error with no parity errors, motivated by the need to correct dual CRC errors, then the design of Hong et al. would produce no

correction, and an error indication to the system. This is identical to the operation of the applicant's claim. Therefore, all of the conditions for the applicant's claim 11 are therefore met in Hong et al. above.

26. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. The Hong et al. patent column 15 lines 53-64 describes the process of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. Not mentioned are the precise steps as outlined in the applicant's claim 12. However, Hong et al. uses the same basis for identifying the errors, and the same logic behind implementing the reconstruction of data (column 23 paragraph 2). Identical methods would be required in order to achieve the same result. On the basis of correcting two simultaneous checksum errors in Hong et al., and the same being claimed by the applicant's claim 12, one skilled in the art at the time of the invention would find the method of Hong et al. and the applicant to be similar. One skilled in the art, motivated to provide an effective dual CRC error method, would have provided the same method for either Hong et al. or the applicant.

27. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. The Hong et al. patent column 15 lines 53-64 describes the process of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since the applicant's claim 13 takes the case of checksum correction,

and the conditions are similar to the conditions that Hong et al. describe in error correction there would be no correction without parity vs. checksum errors. The data loss condition will remain, and will be reported to the system because Hong et al. would be unable to correct both errors. One with ordinary skill in the art at the time of the invention would see that the error condition would remain active, and the data would remain uncorrected, if either of the parity indicators were showing "good" data. If one skilled in the art were to create a flow chart of CRC error correction, motivated by the need to correct dual CRC errors, then the design of Hong et al. would produce the same results, and an error indication to the system. This is identical to the operation of the applicant's claim. Therefore, all of the conditions for the applicant's claim 13 are therefore met in Hong et al. above.

28. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. The Hong et al. patent column 15 lines 53-64 describes the process of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since there would be an error in the second checksum itself, the checksum would be reconstructed in Hong et al. in the same manner that data is reconstructed, and therefore the second data error would be corrected (column 23 paragraph 2). One with ordinary skill in the art at the time of the invention would be motivated to correct one of two CRC errors in the same manner as Hong et al. because of it's simplicity. Hong et al. corrects the checksum under

the conditions described by the applicant's claim 14 and so by providing the same result, teaches the applicant's claim.

29. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. The Hong et al. patent column 15 lines 53-64 describes the process of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also states means for receiving track pointers indicating the presence of errors in ones of said tracks and for disabling the correction apparatus when three or more tracks are in error (see column 40 lines 57-60). In other words, there will be guaranteed through Hong et al. an unconditional error condition reported to the system whenever three or more errors occur while validating the checksums. . However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

30. Claims 16 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Hong et al., in patent column 35 lines 63-68, and column 36 lines 1-27 substantially teaches the method of arranging the data signals, generating check redundancy signals, with a 1$^{st}$ set of

checks bits (CRC type), a 2nd set of parity check bits, storing the data as digital signals, and then detecting an error in at least one of the signals (see also the abstract in Hong et al.). Hong et al. bases the error correction on a horizontal to vertical redundant relationship (column 2 lines 38-48) of bytes and bits. When reading data, the CRC and parity bits are recomputed on the incoming data, and compared with the incoming CRC and parity, and failing data are identified based on unequal comparisons. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

31. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Hong et al., in patent column 35 lines 63-68, and column 36 lines 1-27 substantially teaches the method of arranging the data signals, generating check redundancy signals, with a 1st set of checks bits (CRC type), a 2nd set of parity check bits, storing the data as digital signals, and then detecting an error in at least one of the signals (see also the abstract in Hong et al.). Hong et al. bases the error correction on a horizontal to vertical redundant relationship (column 2 lines 38-48) of bytes and bits. When reading data, the CRC and parity bits are recomputed on the incoming data, and

compared with the incoming CRC and parity, and failing data are identified based on unequal comparisons. When comparing check signals, Hong et al. in the Abstract says that the checksum can be used to locate the error in the data. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

32. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 30 lines 61-65 of Hong et al. fully teaches a system for "...means for correcting errors in all bytes extending along any one channel..." In other words, all blocks are reviewed for errors and more than one byte can be pointed out. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

33. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 29 lines 39-46 of Hong et al. fully teaches a system for "...parity bit generating means...for correcting errors..." In other words, a new parity relationship is generated and can be compared to the original. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

34. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 and in view of Sawao Iwatani, U.S. Patent No. 6023780. In Iwatani's patent, column 40 lines 41-45 of that patent teaches, "...data read controlling means for comparing the data read from said two disk drives and searching, when the data are mismatched..." This identifies the method used to detect errors in two drives is comparison of the data in the two drives directly. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A

person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

35. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. column 30 lines 61-68 fully teaches a system for "...correcting errors in all the bytes along any one channel..." calculating parity and CRC, and if there is an error, pointing to the data in error, and correcting the data associated with the check signal. This applies to checksums in error as well as data in error. In the applicant's claim 23 above, the applicant indicates a checksum correction, which Hong et al. teaches. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

36. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 and in view of Sawao Iwatani, U.S. Patent No. 6023780. In Iwatani's patent, column 41 lines 31-32 of that patent teaches, "...restructuring the data based on the first parity and valid part of the data..." The restructured data is the validated in Iwatani column 41 lines 48-50,

"wherein a cyclic redundancy check is used to validate the restructured data..." The combination of Hong and Iwatani completely covers all of the points of the applicant's claim. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

37. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187, and in view of Ng et al., U.S. Patent No. Re. 36846. Column 37 lines 4-6 of Hong et al. teaches "...showing which signals in such group are in error; and changing the signals in error..." This teaching of Hong, while not specifically teaching the replacement of the checksum, shows that the checksum may be replaced if it is determined to be in error. In RAID systems, replacement of entire blocks because of errors is a common occurrence. In Ng et al., column 37 lines 54-68 and column 38 lines 1-56, the method detects the error, identifies the faulty location, rebuilds the data, and then re-writes the corrected data. If one skilled in the art at the time of the invention were storing data, parity, and checksums, then the re-writing of data would encompass all three parts of the system, including checksums. Though not specific, the combination of these two inventions would have made it obvious.

However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

38. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 26 of this application above. In the Hong et al. patent, column 30 lines 61-68 of that patent teaches the system whereby detecting and correcting up to two errors in the checksum is done by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since there would be no correction without parity errors, the data loss condition will remain, and will be reported to the system. All of the conditions for the applicant's claim 26 are therefore met in Hong et al. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated

to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

39. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 27 of this application above. In the Hong et al. patent, column 30 lines 61-68 of that patent describes the system where there is detecting and correcting of up to two errors in the checksum by identifying the checksums in error using parity pointers. Not mentioned are the precise steps as outlined in the applicant's claim 27. However, Hong et al. uses the same basis for identifying the errors, and the same logic behind implementing the reconstruction of data would be required in order to achieve the same result. On the basis of correcting two simultaneous checksum errors in Hong, and the same being claimed by the applicant's claim 27, one skilled in the art at the time of the invention would assume the claims to be similar. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

40. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 28 of this

application above. In the Hong et al. patent, column 30 lines 52-68 of that patent teaches the system where detecting and correcting up to two errors in the checksum is done by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since the applicant's claim 28 takes the case of checksum correction and compares it to parity, the conditions, which indicate data loss for the applicant, are similar to the conditions that Hong et al. describe. Since there would be no correction without parity vs. checksum errors, the data loss condition will remain, and will be reported to the system. All of the conditions for the applicant's claim 28 are therefore met in Hong et al. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

41. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 29 of this application above. In the Hong et al. patent, column 30 lines 52-68 of that patent teach the system of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since

there would be an error in the checksum itself, the checksum may be reconstructed in the same manner that data is reconstructed. Hong et al. corrects the checksum under the conditions described by the applicant's claim 29 and so by providing the same result, teaches the applicant's claim. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

42. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 30 of this application above. In the Hong et al. patent column 30 lines 52-68 teaches the system of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also states "...means for inhibiting said control signals Q when N1 or N3 is on." (column 30 lines 22-23). In other words, there will be guaranteed through Hong et al. an unconditional error condition reported to the system whenever three or more errors occur while validating the checksums. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would

have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

43. Claims 31- 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to the claims of this application above, and further in view of Sawao Iwatani, U.S. Patent No. 6023780. The claims of Hong et al. and Iwatani, the combination of the two, completely cover all of the points of the applicant's claims in the error handling of redundant storage arrays in a computer medium causing the operation of this system. The rejections recorded in this document in paragraphs 15 to 42, which refer to the system and methods (claims 1 to 30 of the applicant), by association with the applicant's claim of a computer medium, are applied to the applicant's claims 31 – 45. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

44. Claims 46 - 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 29 lines 16-38 of

Hong et al. fully teaches a system of "...arranging data signals and generating check redundancy signals in connection with transferring digital data signals..." which generates a 1st set of check bits (CRC) with a redundant relationship to each of a plurality of channels, and generating 2nd check signals having a parity relationship with single frames of data, each frame a part of a plurality of frames, the parity also having a redundant relationship with the CRC check signal. The relationship of the 1st to the 2nd checks is that of a vertical and horizontal nature with the data block. When reading data, the CRC and parity bits are recomputed on the incoming data, and compared with the incoming CRC and parity, and failing data are identified based on unequal comparisons. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

45. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 29 lines 16-38 of Hong et al. fully teaches a system for "...reading correcting errors in digital signals..." which generates a 1st set of check bits (CRC) with a redundant relationship to each of a plurality of channels, and generating 2nd check signals having a parity relationship with single frames of data, each frame a part of a plurality of frames,

the parity also having a redundant relationship to the CRC check signal. The relationship of the 1st to the 2nd checks is that of a vertical and horizontal nature to the data block. When reading data, the CRC and parity bits are recomputed on the incoming data, and compared with the incoming CRC and parity, and failing data are identified based on unequal comparisons. When comparing check signals, Hong et al. column 30 lines 14-23 teaches that the checksum can be used to locate the error in the data. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

46. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 30 lines 62-63 of Hong et al. fully teaches a system for "...means for correcting errors in all bytes extending along any one channel..." In other words, all blocks are reviewed for errors and more than one byte can be pointed out. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and

the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

47. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 29 lines 39-46 of Hong et al. fully describes a system for parity bit generating means, for correcting errors. In other words, a new parity relationship is generated and can be compared to the original. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

48. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187, and in view of Sawao Iwatani, U.S. Patent No. 6023780. In Iwatani's patent, column 40 lines 41-45 of that patent teaches, "...data read controlling means for comparing the data read from said two disk drives and searching, when the data are mismatched..." This identifies the method used to detect errors in two drives is comparison of the data in the two drives directly. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs

along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

49. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187. Column 30 lines 62-63 of Hong et al. fully teaches a system for "...correcting errors in all the bytes along any one channel...", calculating parity and CRC, and if there is an error, pointing to the data in error, and correcting the data associated with the check signal (column 29 lines 15-46). This applies to checksums in error as well as data in error. In applicant's claim 53 above, the applicant indicates a checksum correction, which Hong et al. teaches. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

50. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 54 of this

application above, and further in view of Sawao Iwatani, U.S. Patent No. 6023780. In Iwatani's patent, column 41 lines 29-30 of that patent teaches, "...restructuring the data based on the first parity and valid part of the data..." The restructured data is then validated in Iwatani column 29 lines 48-52, "wherein a cyclic redundancy check is used to validate the restructured data..." The combination of Hong and Iwatani completely covers all of the points of the applicant's claim. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

51. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187, and in view of Ng et al., U.S. Patent No. Re. 36846. Column 37 lines 4-6 of Hong et al. teaches, "...showing which signals in such group are in error; and changing the signals in error..." This teaching of Hong, while not specifically teaching the replacement of the checksum, shows that the checksum may be replaced if it is determined to be in error. In RAID systems, replacement of entire blocks because of errors is a common occurrence. In Ng et al., Figure 11 and column 10 lines 11-27, the method detects the error, identifies the faulty location, rebuilds the data, and then

re-writes the corrected data. If one skilled in the art at the time of the invention were storing data, parity, and checksums, then the re-writing of data would encompass all three parts of the system, including checksums. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

52. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 56 of this application above. In the Hong et al. patent, column 30 lines 61-68 of that patent teaches the system whereby detecting and correcting up to two errors in the checksum is done by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since there would be no correction without parity errors, the data loss condition will remain, and will be reported to the system. All of the conditions for the applicant's claim 11 are therefore met in Hong et al. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and

the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

53. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 57 of this application above. In the Hong et al. patent, column 30 lines 61-68 of that patent teaches the system where there is detecting and correcting of up to two errors in the checksum by identifying the checksums in error using parity pointers. Not mentioned are the precise steps as outlined in the applicant's claim 57. However, Hong et al. uses the same basis for identifying the errors, and the same logic behind implementing the reconstruction of data would be required in order to achieve the same result. On the basis of correcting two simultaneous checksum errors in Hong, and the same being claimed by the applicant's claim 57, one skilled in the art at the time of the invention would assume the claims to be similar. And one would have been motivated at the time of the invention to utilize the method of Hong et al. and apply it towards a block-wise data system. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to

block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

54. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 58 of this application above. In the Hong et al. patent, column 30 lines 52-68 describe the system where detecting and correcting up to two errors in the checksum is done by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since the applicant's claim 58 takes the case of checksum correction and compares it to parity, the conditions, which indicate data loss for the applicant, are similar to the conditions that Hong et al. describe. Since there would be no correction without parity vs. checksum errors, the data loss condition will remain, and will be reported to the system. All of the conditions for the applicant's claim 58 are therefore met in Hong et al. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

55. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 59 of this

application above. In the Hong et al. patent, column 30 lines 52-68 teach the system of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also infers that correction of checksums does not occur if there are no parity indicators. Since there would be an error in the checksum itself, the checksum may be reconstructed in the same manner that data is reconstructed. Hong et al. corrects the checksum under the conditions described by the applicant's claim 59 and so by providing the same result, teaches the applicant's claim. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

56. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Se J. Hong et al., U.S. Patent No. Re. 30187 as applied to claim 60 of this application above. In the Hong et al. patent, column 30 lines 52-68 teach the system of detecting and correcting up to two errors in the checksum by identifying the checksums in error using parity pointers. It also states "...means for inhibiting said control signals Q when N1 or N3 is on." (column 30 lines 23-24). In other words, there will be guaranteed through Hong et al. an unconditional error condition reported to the system whenever three or more errors occur while

validating the checksums. However, the Hong et al. teachings are directed towards bytes, where the applicant deals with data blocks. Also, cyclic redundancy runs along the horizontal plain in Hong et al., and the parity lies in the vertical. One with ordinary skill in the art at the time of the invention would have seen this obvious comparison between the applicant's and the Hong et al. claims. A person ordinarily skilled in the art at the time, motivated to apply error correction to block-wise data, would have used the teachings of Hong et al. to specify multiple error correction capabilities.

***Conclusion***

57. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

John P Trimmings
Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Art Unit 2133

jpt